

## B. E.

Fourth Semester Examination, May-2007

# COMPUTER ARCHITECTURE & ORGANIZATION

**Note :** Attempt any five questions. All questions carry equal marks.

**Q. 1.** Design a combinational circuit with three inputs x, y, z and three outputs A, B, C. When the binary input is 0, 1, 2, 3 the binary output is one greater than the input when the binary point is 4, 5, 6 or 7, the binary output is one less than the input.

**Ans.**

Input			Next state		
X	Y	Z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

J <sub>3</sub>	K <sub>3</sub>	J <sub>2</sub>	K <sub>2</sub>	J <sub>1</sub>	K <sub>1</sub>
0	x	0	x	1	—
0	x	1	x	x	1
0	x	x	0	1	x
1	x	x	1	x	1
x	1	1	x	1	x
x	0	0	x	x	1
x	0	x	1	1	x
x	0	x	0	x	1

x \ yz	00	01	11	10
0	1 0	d 1	d 3	1 2
1	1 6	d 5	d 7	1 6

x \ yz	00	01	11	10
0	d 0	1 1	1 3	d 2
1	d 4	1 5	1 7	d 6

yz \ x	00	01	11	10
0	0	1	d	d
1	1	0	d	d

$$J_2 = \bar{x}z + x\bar{z}$$

yz \ x	00	01	11	10
0	d	d	1	0
1	d	d	0	1

$$\bar{x}z + x\bar{z} = k_2$$

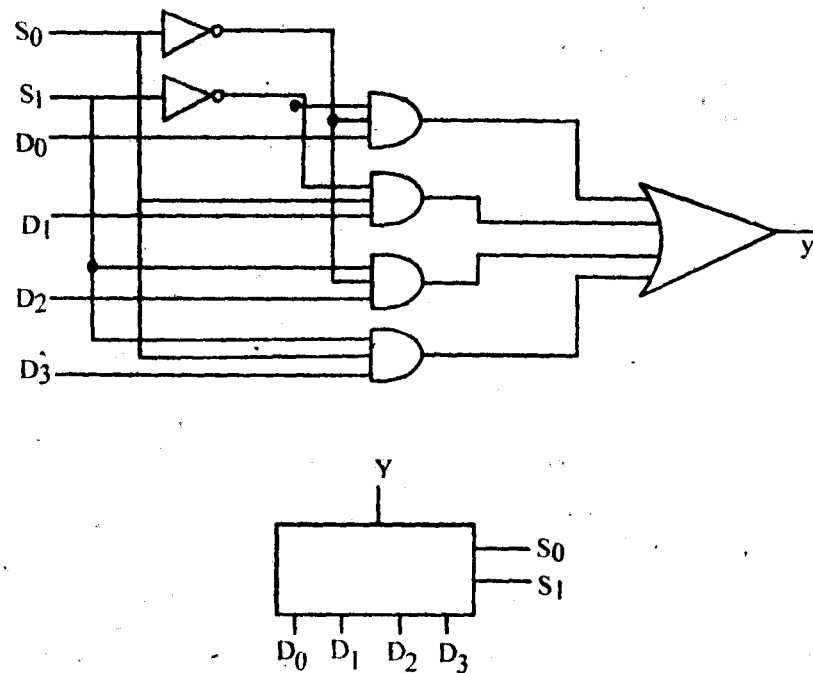
yz \ x	00	01	11	10
0	0	0	1	0
1	d	d	d	d

$$J_3 = yz$$

yz \ x	00	01	11	10
0	d	d	d	d
1	1	0	0	0

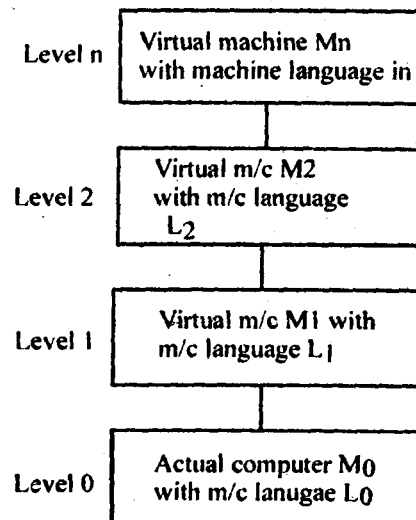
$$k_3 = \bar{y}\bar{z}$$

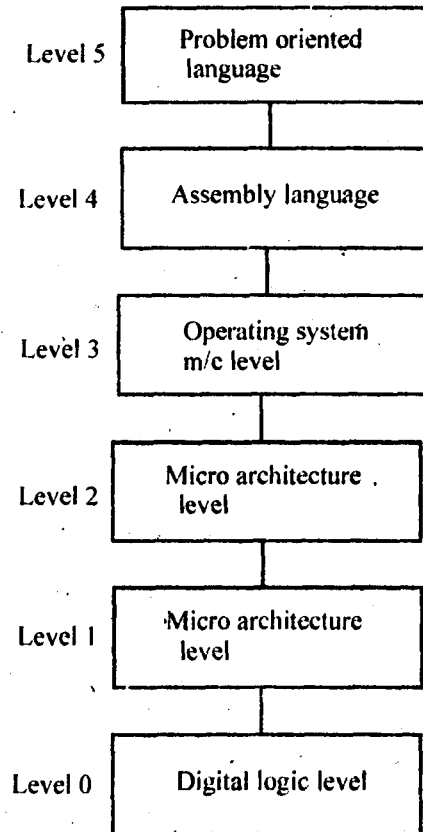




**Q. 2. (a) Draw and explain the multilevel viewpoint of a machine.**

**Ans. Multilevel View Point :** The computers are designed as a series of levels, each one built to its predecessor. Each level represents a distinct abstraction with different objects and operations, the set of data types, operations and features of each level is called its architecture. The architecture deals with those aspects that are visible to the user of that level.





Lowest three levels are intended for running interpreter and translator and upper three levels are intended for application program.

**Q. 2. (b) What are the various types of operating systems? Discuss the characteristics of each briefly.**

**Ans.** An operating system is an interface between the computer and programmer. There are following types of operating systems :

**1. Time Sharing :** In this, it has following characteristics.

Interactive use of a computer.

Several users can share the computers simultaneously.

**2. Distributed Operating System :**

- \* It has distributed file system.
- \* Common between processes in the distributed system through
- \* Remote procedure call

- \* Group communication.
- \* Process in load balancing way.

**3. Simple Batch System :** Sequence jobs and transfer control automatically from job to job.

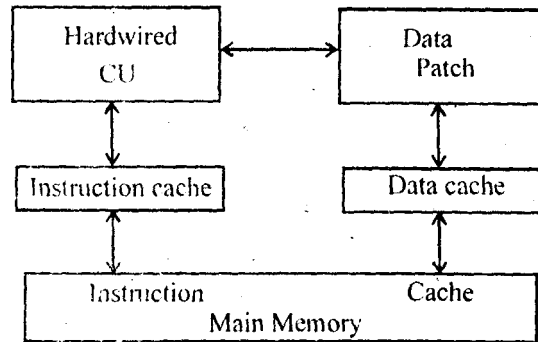
- \* Monitor the current job.
- \* Device drivers.

**4. Multiprogramming System :** It has OS and several jobs in memory.

- \* When one job waits for completion of an input/output operation—another is executed.
- \* Issues related to the system are protection and some scheduling.

**Q. 3. (a) What are the characteristics of RISC computers?**

**Ans. RISC Computers :** RISC computers are also called hardwired control systems. It has small set of instructions and most of them are register based. The addressing modes used for this system are limited to 3-5. It has large numbers of general purpose registers mostly with split cache.



**Q. 3. (b) Why a number of addressing modes are needed? By taking suitable examples explain the following addressing modes :**

- Direct
- Indexed
- Relative
- Immediate
- Register

**Ans. Addressing Modes :** The addressing mode specifies a rule for interpreting or modifying the address field of the instruction before the operand is actually referenced. The operational field of an instruction specifies the operation to be referenced.

**1. Direct Mode :** In direct mode, the effective address is equal to the address part of the instruction operand in memory and its address gives by address field of instruction.

**2. Indexed :** In this mode, the contents of index register is added to address part of instruction.

**3. Relative :** To define E. A we add program counter contents and address part of instruction.

**4. Immediate :** In this operands are in instruction itself and it has operand field rather than address field.  
eg. MVI A, 06.

**5. Register :** In this mode, operands are in the registers. The particular registers are selected from a register field in the instruction.

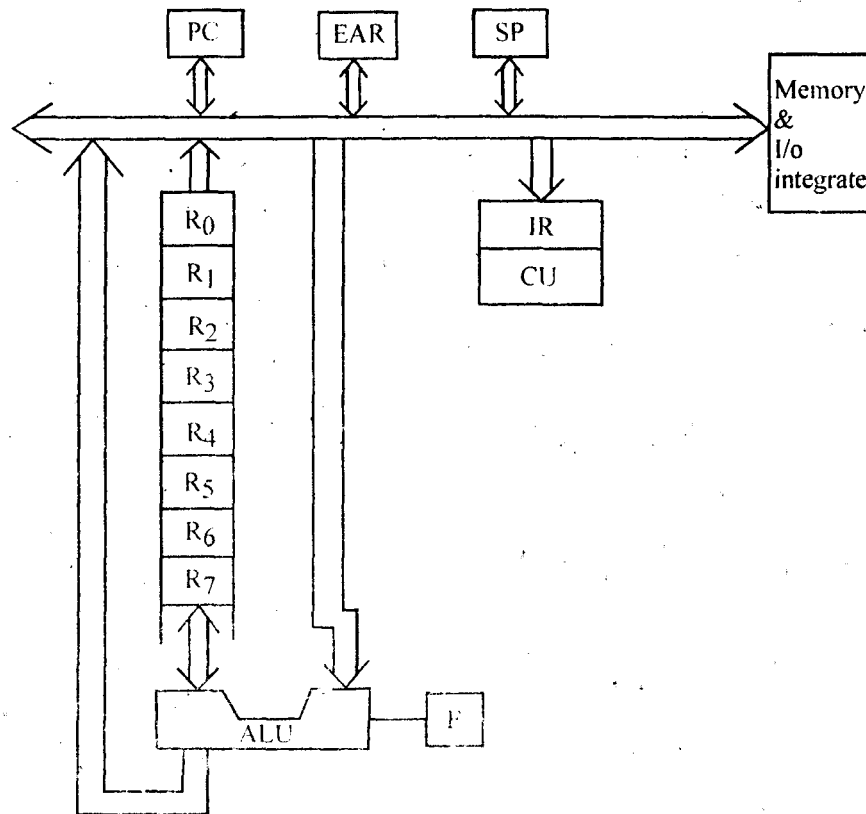
**Q. 4. Draw and explain the detailed data path for a register based CPU and stack based CPU.**

**Ans. CPU Architecture :** The selection of an instruction set for a computer depends on the manner in which CPU is organised. The discussion of register based CPU and stack based CPU architecture.

**1. Register Based CPU :** In this type of CPU, multiple registers are used as accumulator. Such a CPU has a general purpose register organisation. The use of registers results in short program with limited instructions.

**Advantages :**

1. It results in shorter program size than an accumulator based CPU.
2. It requires memory locations for storing partial results. Hence, additional memory accesses are needed during program execution.
3. Increase in number of registers increases CPU efficiency.



**Disadvantages :**

1. Use of unnecessary registers create problems.
2. Computer do not work efficiently in case of more registers.

**Stack Based CPU :** Stack is a LIFO data structure. It stores the operands. It is present inside the CPU or a portion of memory can be used as a stack. A register is used to point to the address of top location of the stack. The register is called stack pointer. When item is stored in the stack it is called PUSH operations and when item is removed from the stack it is called POP operation.

**Advantages :**

1. Easy programming and high efficiency of computers.
2. Highly suited for block structured language.
3. Instructions do not have address field.

**Disadvantages :**

1. Additional hardware circuitry needed for stack implementation.
2. Increased program size.

**Q. 5. (a) Define the term "locality of reference." How this concept is used in the design of memory system?**

**Ans. "Locality of Reference" :** Memory hierarchy was developed based on program behaviour known as locality of reference. There are 3 dimension of locality of reference.

1. Temporal 2. Spatial 3. Sequential.

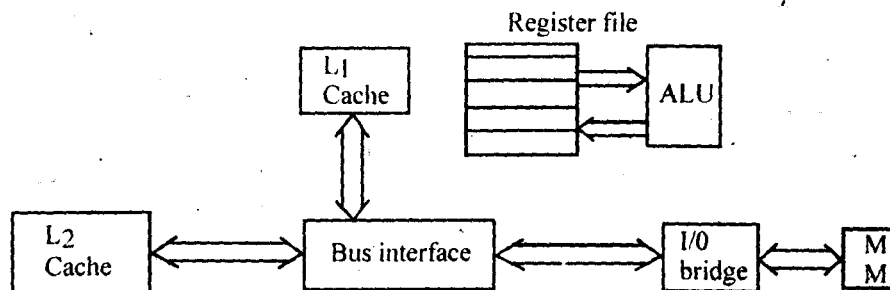
**1. Temporal :** Recently referenced items are likely to be referenced again in near future e.g. program construct, iterative loops etc.

**2. Spatial :** It refers to the tendency for a process to access address near one another eg. operations on tables, arrays involves access of certain cluster etc.

**3. Sequential :** In Typical programs, the execution of instructions follows a sequential order or the program order, unless a branch instruction out-order-execution.

**Q. 5. (b) What do you mean by cache memory? Draw and explain the block diagram of cache memory.**

**Ans. Cache Memories :** Cache memories are small, fast SRAM based memories managed automatically in hardware. It holds frequently accessed blocks of main memory CPU looks first for data in L1 then in L2 then in main memory. The typical bus structure is given below :





If the particular word we are searching found in cache we call it hit otherwise miss.

The most heavily used memory words are kept in the cache when CPU needs a word, it first looks in the cache. If the word is not there it then goes to the main memory. If the substantial fraction of the word are in cache, the average access time is greatly reduced.

**Basic Characteristics of Cache :** It has fast access time, therefore, little or no time must be wasted on searching a word in cache.

**Mapping Process :** The transformation of data from main memory to cache memory is called mapping process. There are 3 types of mapping for cache,

- Associative mapping
- Direct
- Set associative.

**Q. 6. (a) State and explain the Amdahl's law.**

**Ans. Amdahl's Law :** This law is basically based on fixed work, load and problem size. For each time period the number of processors used to create program (is defined as DOP (degree of Parallelism).

It is a law generating the speed up of parallel processors versus using only one processor. It is used to find the maximum expected improvement to the overall system, when only a part of system is improved. Speed up of the program is the time it takes the program to execute.

$$\text{Speed up} = \frac{T(1)}{T(n)}$$

$$\text{Eff:} = \frac{\text{Speed up}}{\text{No. of processors}}$$

Now suppose serial part of program is performed in  $B \cdot T(1)$  times then the parallel part will be performed in  $\frac{(1-B) \cdot T(1)}{N}$ .

New speed up

$$S = \frac{N}{(B \cdot N) + (1 - B)}$$

The factors that decrease the speed are :

1. Computational latency
2. Memory access delay

$$S_n = \frac{T(1)}{T(n) + Q_n}$$

**Q. 6. (b) How the throughput of a system can be enhanced with parallel mechanisms?**

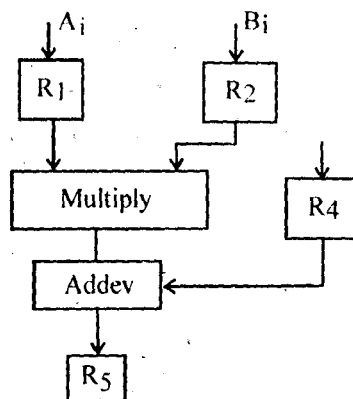
**Ans.** Pipelining is a general techniques for increasing the processor throughput without requiring large amount of hardware. It is a process of decomposing a sequential process into suboperations with each sub-process being executed in a special dedicated segment that operate concurrently with all other segments.

A pipeline can be visualized as a collection of processing segment through which binary information flows. Each segment performs partial processing dedicated by the way the task is partitioned. The final result is obtained when data has passed through all segments.

$$A_i * B_i + C_i \text{ where } i = 1, 2, \dots, 7.$$

$$R_1 \leftarrow A_i, R_2 \leftarrow B_i, R_2 \leftarrow R_1 * R_2$$

$$R_4 \leftarrow C_i, R_5 \leftarrow R_3 + R_4.$$



**Q. 7. (a) What do you mean by control memory? How is it different than simple memory?**

**Ans.** It is a method of control unit design in which control signal selection and sequencing information is stored in ROM and RAM is called control memory. The control signals are activated any time specified by microinstruction which is fetched from control memory is same way instructions is fetched from memory. Each micro instructions also explicitly or implicitly specify next micro instructions to be used. Simplest form of microinstruction has 2 parts.

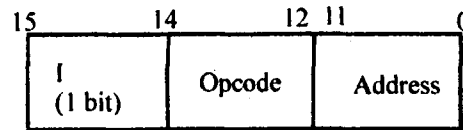
1. **Control Field** : Specify control signals to be activated.
2. **Address Field** : Specify address is can of next microinstruction to be executed.

**Q. 7. (b) What are the various types of instructions supported by the 8086 family. Discuss each briefly.**

**Ans. Instructions Set Format** : It defines the layout of bits of instructions in terms of its constituent part an instruction format must include an opcode and implicitly or explicitly 0 or more operands.

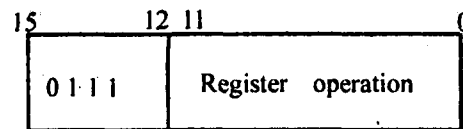
The basic computer has 3 instruction code formats having 16 bits.

### 1. Memory Reference Instruction :

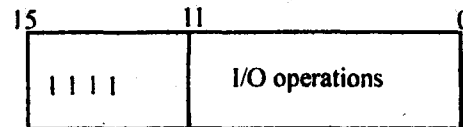


It uses 12 bits to specify address and one bit to specify addressing mode.

**2. Register Reference Format :** A register reference instruction is recognised by a code 111 with 0 in MSB.



**3. Input/Output Instruction :** Input/output instructions do not need a reference to memory and is recognized with operations code with a 1 in left most bit of instruction.



**Q. 8. (a) What are the various parameters that can be used to evaluate the performance of a memory unit.**

**Ans.** Parameter are as follows :

- 1. Speed :** The major parameter to find the performance of any memory unit is speed. It can be calculated as number of bits processed per second.
- 2. Cost :** The cost is the other factor. The cost of device increases as the size increases.
- 3. Size :** Size can be measured in bytes, MG, GB etc.
- 4. Efficiency :** Efficiency is the other factor to find out the performance of memory unit.

**Q. 8. (b) What do you mean by structure organization?**

**Ans. Structured Organization :** It is a way of structuring computers as a series of abstractions, each abstraction building on the one below it. In this way, complexity is mastered and computer system is designed in a systematic and organised way. Programs written in  $L_1, L_2, \dots, L_n$  can either interpreted by interpreter running on covers machine or translated to other language. Corresponding to lower level by the translator. The structured organisation involves,

1. CPU
2. Cache
3. Main memory
4. Secondary memory
5. Input/output units.

